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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/878,554	06/11/2001	Xinghao Chen	FIS920010060US1	5168

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ORRICK, HERRINGTON & SUTCLIFFE, LLP
IP PROSECUTION DEPARTMENT
4 PARK PLAZA
SUITE 1600
IRVINE, CA 92614-2558

EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 10/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/878,554	CHEN ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,6 and 8-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,6 and 8-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 2, 6 and 8-13 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 2 and 8-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Snethen; Thomas J. (US 3961250 A).

35 U.S.C. 102(b) rejection of claims 2 and 8-10.

Snethen teaches a. performing a good machine simulation on the IC with the test to obtain values of each internal node of the IC (col. 5, lines 19-22 in Snethen teach a Simulator 600 in Figure 3 for simulating the Device Under Test [DUT] 84 referred to as a network under test; col. 4, lines 18-21 in Snethen teach that the DUT logic networks to be tested is an IC; col. 19, lines 30-35 in Snethen teach that Simulator 600 includes a good logic model, i.e., a good machine simulation for performing a good machine simulation on the DUT logic network IC; col. 19, lines 60-65 in Snethen teach that the

predicted state for any logic block in the network is obtained; Figure 3B in Snethen teaches that state values include information on input and output nodes of the internal blocks; hence Snethen teaches performing a good machine simulation on the DUT logic network IC 84 with a test to obtain predicted state values comprising information on input and output nodes of each internal block of the IC; Note: col. 2, lines 53-56 in Snethen teach that a binary value of a point or node within the DUT logic network IC 84 that is opposite from that expected in the absence of the assumed fault is referred to as a test value or test pattern); b. based on the good machine simulation, identifying the potential faults to be tested by the test by backtracing, in a single detection pass, through logic gates and memory elements of the IC, starting at each observable node, said backtracing being based on outputs of said logic gates and memory elements, the outputs being obtained from said good machine simulation (col. 2, line 39-56 in Snethen teach that simulation is used to generate a test value or a test pattern and col. 2, line 57-68 to col. 3, lines 1-9 teach that assumed or potential faults in the actual DUT logic network IC 84 are detected by backtracing through the actual DUT logic network IC 84 to find particular desired changes to the test pattern of binary valued signals applied to the primary inputs and comparing the binary values of the primary outputs of the actual logic network under test with the primary outputs of the simulated logic network) and, said backtracing being limited to paths along which a faulty value has a possibility of propagating to said observable node (the Abstract in Snethen teaches a "test value for this assumed specific fault in the simulated network is then propagated towards a primary output, one logic stage at a time, by backtracing through the network to a

primary input to determine which primary input value must be altered in order to propagate the assumed fault towards a primary output"); c. with the test, performing the fault simulation on the potential faults to be tested; and repeating steps a through c for additional tests of the plurality of tests (col. 2, lines 62-68 in Snethen teaches that a series of test patterns is generated by repeating Steps a to c).

Note: inaccessible nodes in col. 1, lines 39-40 in Snethen are potential faults in the IC that are blocked from being observed.

Note: col. 4, lines 15-35 in Snethen teach the use of generl purpose computer for utilization in testing and simulation (see Figure 1 in Snethen).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 6 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Snethen; Thomas J. (US 3961250 A) in view of Abramovici; Miron et al. (US 5896401 A, hereafter referred to as Abramovici).

35 U.S.C. 103(a) rejection of claims 6 and 11-13.

Snethen substantially teaches the claimed invention described in claim 2 (as rejected above).

However Snethen does not explicitly teach the specific use of processing by the fault simulation by starting the backtraces from only observable nodes wherein the faults to be tested were detected.

Col. 6, lines 37-52 in Abramovici, in an analogous art, teaches observed results of stem analysis during the test further limit a number of faults requiring processing by the fault simulation by recognizing that is not always necessary to propagate the fault effects of stems "all the way" to POs and by starting the backtraces from only observable nodes wherein the faults to be tested were detected, for example, from node F as taught in col. 6, lines 37-52 of Abramovici.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Snethen with the teachings of Abramovici by including use of processing by the fault simulation by starting the backtraces from only observable nodes wherein the faults to be tested were detected. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of

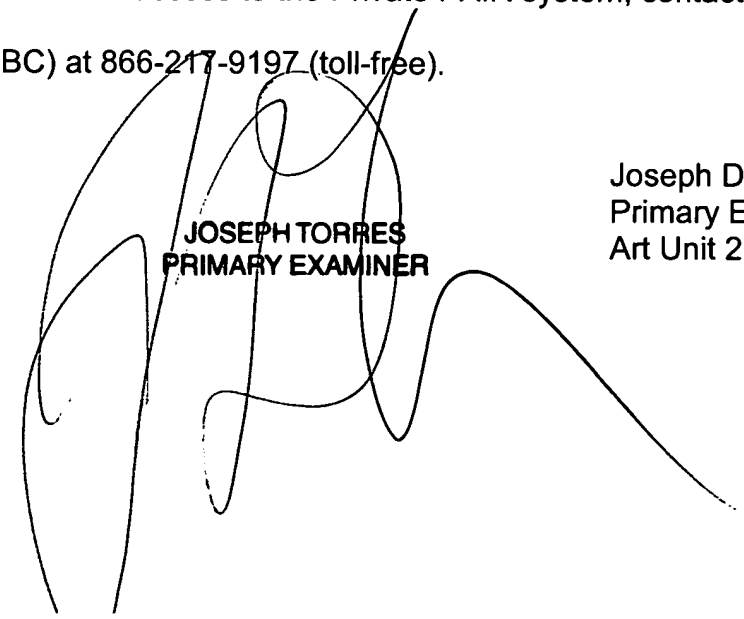
processing by the fault simulation by starting the backtraces from only observable nodes wherein the faults to be tested were detected would have provided the opportunity to improve processing time (col. 6, lines 37-52 of Abramovici).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133